But, with the high-k dielectric layer 14 described above in accordance with the present invention, the crystallization temperature of the high-k dielectric layer 14 can be increased compared to the prior art, thus reducing leakage current. Here, 2 angstroms is a basic thickness of one atomic layer, and 60 angstroms represents an upper thickness limit that prevents a popping phenomenon during a subsequent annealing process. As is known in the art, hydroxyl radicals trapped in dielectric layers during the formation can pop therefrom upon subsequent annealing, thereby damaging, e.g. leaving a hole in the dielectric layers. If such a popping phenomenon occurs, subsequent processing steps such as gate poly deposition can be significantly inhibited.

On page 11, lines 2-9

Further referring to FIG. 5, even though the amount of the flatband voltage shift is 0 volt, the transconductance of the MOS structure including the Al_2O_3 layer is still less than that of the reference MOS structure. This difference is due to the interface trap density. The interface trap density can be calculated using a charge pumping current shown in FIG. 6, which shows the charge pumping current of SiO_2 and Al_2O_3. As can be seen, the interface trap density of Al_2O_3 is greater than SiO_2. Such interface trap density can be reduced by introducing the metal silicate interface layer 12 between the silicon substrate 10 and the high-k dielectric layer 14.

IN THE CLAIMS

19. (Amended) The multi-layer structure of claim 13, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

25. (Amended) The multi-layer structure of claim 20, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

30. (Amended) The method of claim 29, wherein the upper most layer of the high-k dielectric layer is Al_2O_3.

42. (Amended) A transistor comprising:

a substrate;